REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-32 are in the case. Claims 1, 13 and 14 have been amended. Claims 25-32 have been added. The Specification has been amended to correct several minor informalities.

Regarding the rejection of Claims 1, 13, 2-8, 10-12, 14-20 and 22-24 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Dighe et al. in view of Hwang, independent Claims 1 and 13 have been amended to overcome the rejection. Claim 1 now recites an ATM module including a plurality of data ports, a function module and an ATM processor coupled to each of the data ports and the function module and operably configured to switch ATM data cells to and from the data ports and the function module *without reassembling the ATM data cells into PDUs.* Similarly, Claim 13 now recites am ATM system including a plurality of data ports, a function module and an ATM processor coupled to each of the data ports and the function module and operably configured to switch ATM data cells to and from the data ports and the function module *without reassembling the ATM data cells into PDUs.* This results in a significant improvement in the efficiency of data transmission in ATM modules, especially those configured as switches (between ports) as well as bridges. This improvement permits, as disclosed in the primary embodiment discussed in the Specification, an ATM module that performs both a LAN/WAN bridge function, i.e., the classic router functionality at OSI Layer 3, as well as a switch function between multiple ports at the OSI Layer 2.

By contrast, both Dighe et al. and Hwang disclose configurations that are merely bridges, and both require reassembly of the AAL PDU in packet memory. Both would require scheduling of the AAL PDU to be transmitted, and segmentation of the AAL PDU into ATM cells before transmission in any configuration allowing switching between ports. The other art of record is even less relevant.

Note that in a preferred embodiment of the claimed invention, a packed data structure processor is provided in the ATM processor, that is programmed to control ATM data cell communication, including virtual path cross-connect, quality-of-service, and operation and maintenance functions of such control. (See, for example, Specification at page 21, line 10 through page 22, line 10.) This aspect is called out in new Claims 27 and 31. This allows the ATM processor to operate directly on the ATM data stream (i.e., the OSI Layer 1/2). This, in turn, allows highly efficient switching and bridging of ATM telecommunications traffic, thereby allowing a truly configurable (i.e., port configurations) ATM module. This aspect is called out in new Claims 28 and 32. For example, the ATM processor is able to configure a given port to be a LAN port or a WAN port, allowing considerable flexibility in the use of such an ATM module. Key in this is the configuration of the ATM processor to switch ATM data cells to and from the data ports and the function module *without reassembling the ATM data cells into PDUs.*

It is respectfully submitted that for the above reasons Claims 1 and 13 as now amended are allowable over Dighe et al., Hwang and, indeed over all of the art of record, whether considered individually or in any combination. All of the other claims in the case, including new Claims 25-32, depend, either directly or indirectly from Claim 1 or Claim 13 and so are allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

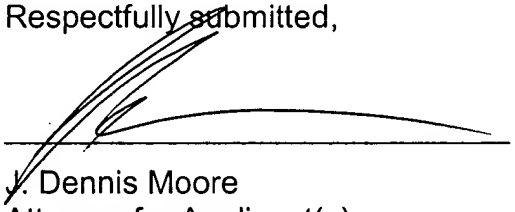
It is respectfully noted that in new Claims 25, 26, 29 and 30, an aspect of a preferred embodiment of the cell buffer module is called out, in that it is configured to store ATM data cells on a priority basis, further preferably being a cache memory. By having the ability to assign priority to different data flows (e.g., connections for an ATM network), and ATM module can support traffic shaping and quality-of-service, and, although not explicitly discussed in the Specification, nonetheless also prevent head of line blocking. Note that these claims recite the storage of ATM data cells on a priority basis, not the storage of PDUs on a priority basis. This is different from Hwang's packet memory.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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